semiconductor substrate.

--30. A device according to claim 27, wherein at least one of said first and second gate electrodes is formed by a damascene gate process.

31. A device according to claim 27, wherein said first insulator film is thinner than said second insulator film, said first transistor is included in a logic circuit, and said second transistor is included in a memory cell.

32. A device according to claim 27, wherein said first and second gate electrodes are connected to each other through a connection layer and top surfaces of said first and second gate electrodes and said connection layer are coplanar.--

REMARKS

Prior to the examination of this application, please enter the above amendments.

If there is any fee due in connection with the filing of this Preliminary Amendment, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

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Dated: October 17, 2000

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